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Application Note

Using the HI1175 Evaluation Board

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Description

The HI1175 evaluation board can be used to evaluate the performance of the HI1175 8-bit 20MSPS analog-to-digital converter (ADC). The board includes clock driver circuitry a reference voltage generator, and a choice of input drive circuitry.

HI1175 Theory of Operation

As illustrated in the functional block diagram of the HI1175, the part is a 2-step ADC converter featuring a 4-bit upper comparator group and two lower comparator groups of 4-bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type CMOS comparator that operates synchronously with the external clock. The operating modes of the part are input sampling (S), hold (H), and compare (C).

The operation of the part is depicted in the timing diagram of Figure 1. A reference voltage that between V_{RT} and V_{RB} is constantly applied to the upper 4-bit comparator group. The analog input is sampled, $V_I(1)$, with the falling edge of the first clock by the upper comparator group. The lower block A also samples the analog input, $V_I(1)$, on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. The lower comparator blocks A and B alternate generating the lower data in order to increase the overall ADC sampling rate.

Layout and Power Supplies

The HI1175 evaluation board is a three layer board with a layout optimized for the best performance for the ADC. Figure 8 through Figure 12 include a schematic of the board, a board layout, and the various board layers. The user should feel free to copy the layout in their application.

In order to avoid latchup of the HI1175 at power up, it is necessary that AV_{DD} and DV_{DD} to the converter be driven from the same supply. The supplies to the board should be driven by individual clean linear regulated supplies. They can be hooked up with external 16 gauge wires to the holes marked +5V, +12V, -12V, and GND on the prototype area. Do not tie the supply grounds together back at the supplies as this will create a ground loop and create additional noise.

Table 1 lists the operating conditions for the power supplies.

TABLE 1. POWER SUPPLIES

POWER SUPPLY	MIN	TYP	MAX	TYP CURRENT
+5V	+4.75V	+5.0V	+5.25V	60mA
+12V	-	+12.0V	-	21mA
-12V	-	-12.0V	-	11mA

Reference Circuit

For the following discussion, refer to the board schematic and the board layout drawing.

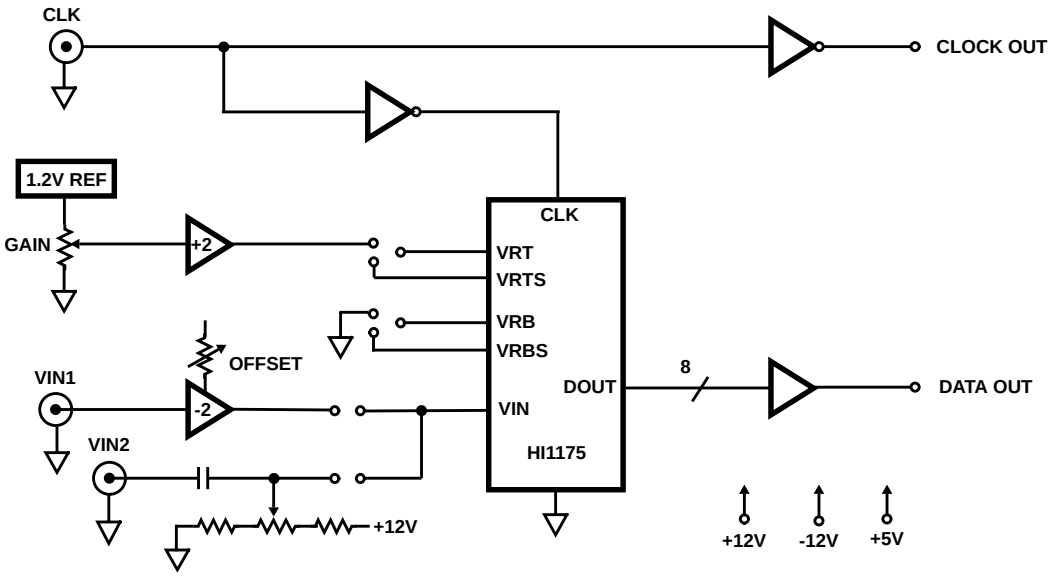
The HI1175 requires two reference voltages: V_{RT} and V_{RB}. The evaluation board provides the user with two options for supplying these voltages. First, by installing jumpers JP3 and JP5, the internal bias generators on the part can be used to generate a V_{RT} of about 2.6V and a V_{RB} of about 0.6V. These generators are resistors to V_{DD} and V_{SS} which in combination with the internal reference resistor string generates the desired voltages.

The evaluation board also provides an external reference that can be applied to the part by installing jumpers JP4 and JP6. In this case an ICL8069 reference diode generates a 1.2V that is gained up by an op-amp to the reference voltage V_{RT} for the ADC. V_{RT} should be kept below 2.8V. R_2 is adjusted at the factory for a V_{RT} reference voltage of +2V ±2mV. V_{RB} is set to GND through JP6.

Analog Input

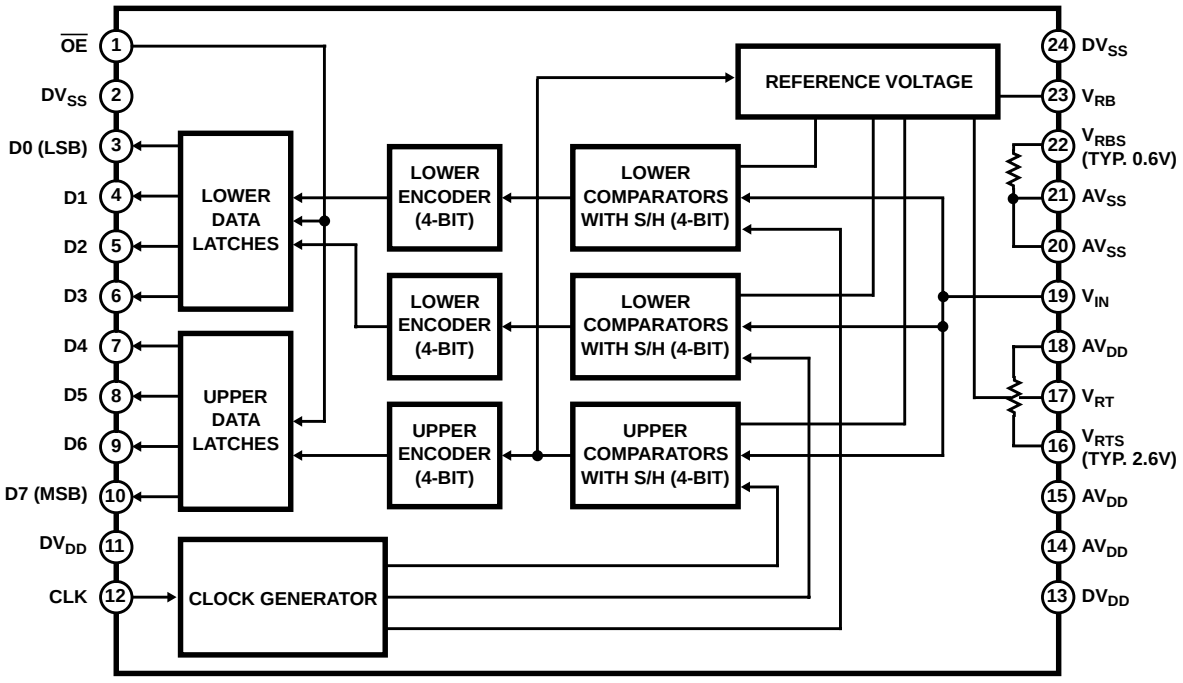
The analog input to the HI1175 can be configured in various ways depending on the input signal and the required level of performance. A signal voltage with a maximum span of V_{RT} - V_{RB} can be AC coupled to the HI1175 through the VIN2 BNC and applied to the ADC by installing jumper JP2. R11 should be adjusted to center the signal in the range of the HI1175.

Evaluation Board Block Diagram



Functional Block Diagram

HI1175



Timing Diagrams

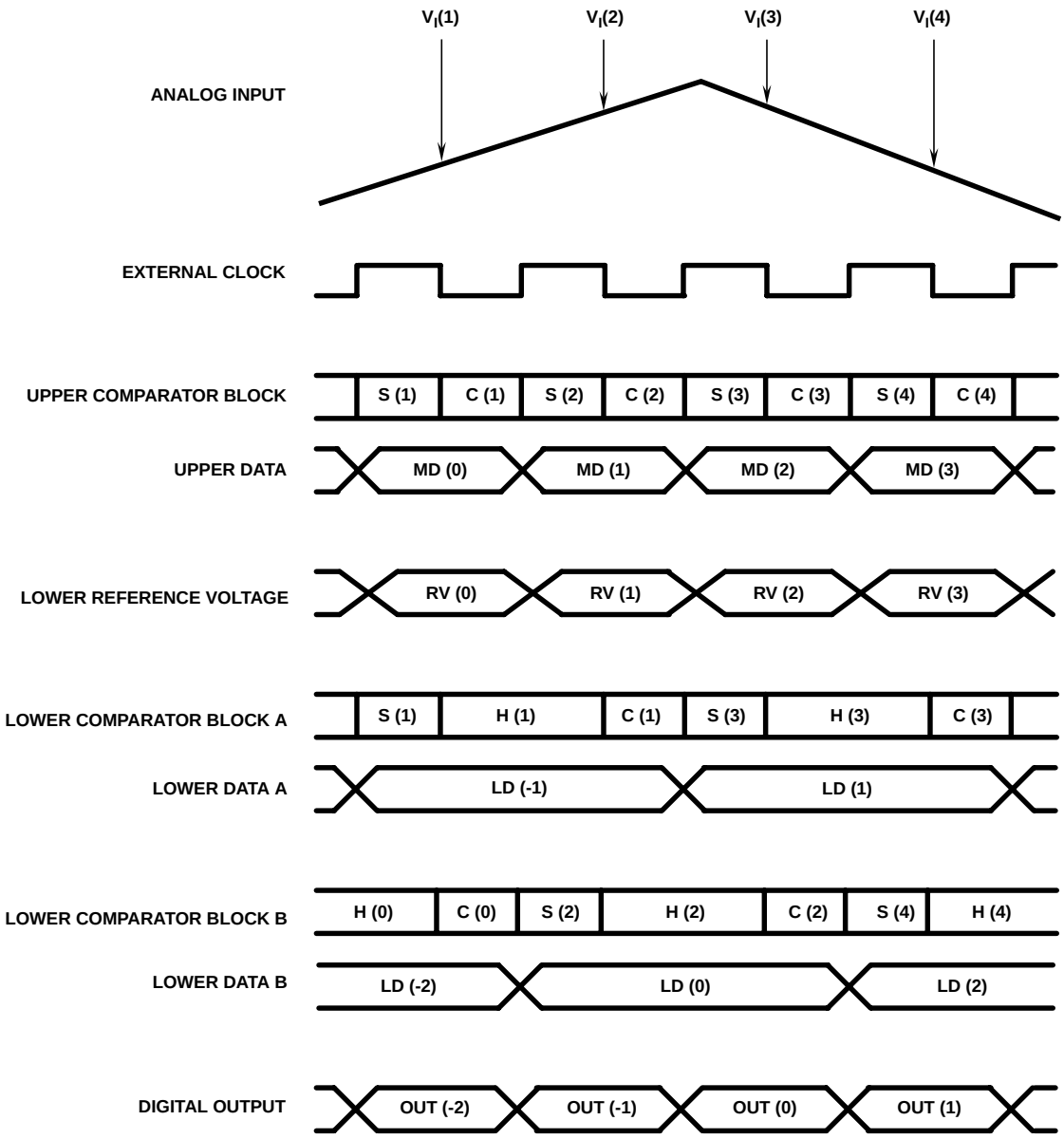


FIGURE 1.

An HA5020 buffer is also provided that can be used to drive the part by inserting JP1. Using Figure 2, the gain of the circuit can be calculated from:

$$V_{OUT} = \left(-\frac{R_9}{R_7}\right) \times V_{IN} - \left(\frac{R_9}{R_6 + R_{15}}\right) \times V_{OFFSET}$$

The signal gain has been set to about negative two. R15 has been adjusted at the factory so that for +0.5V on VIN1 the input to the ADC will be at 0V ±2mV.

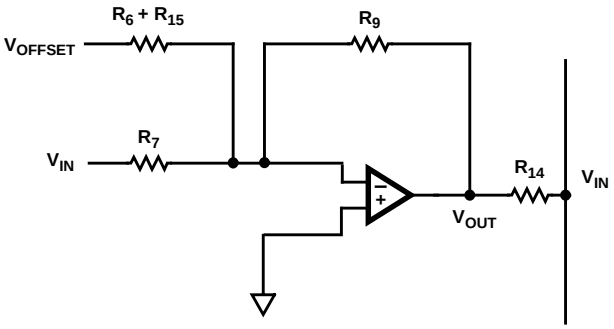


FIGURE 2. INVERTING AMPLIFIER

The circuit in Figure 3 could be used if a negative voltage is not available to provide the offset voltage. V_{OFFSET} could be generated from the 1.2V reference voltage. The gain can be calculated from:

$$V_{OUT} = -\left(\frac{R_3}{R_4}\right) \times V_{IN} + \left(1 + \frac{R_3}{R_4}\right) \times \left(\frac{R_1}{R_1 + R_2}\right) \times V_{OFFSET}$$

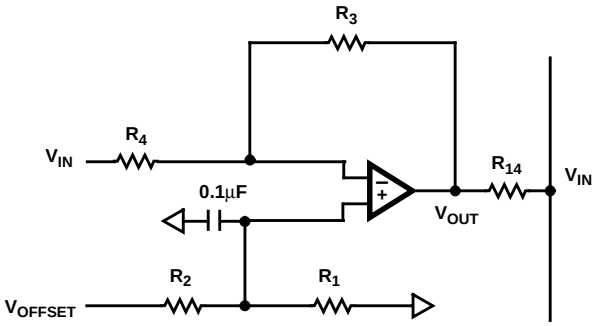


FIGURE 3. MODIFIED BUFFER

The HI1175 could latchup if the analog input exceeds the absolute max input voltage rating. To avoid this resistor R_{14} should be increased to limit the input current to less then 15mA. However, increasing R_{14} beyond what is presently in the evaluation board might sacrifice some AC performance.

The combination of the buffer and the external reference will give the best performance for the HI1175 and allow the most flexibility when dealing with various types of input signals. If an application is extremely cost sensitive then the internal bias generators along with the AC coupled version of the input circuit can be used.

Increased Accuracy

Further calibration of the ADC can be done when using the external reference and input buffer circuit. First, a precision voltage equal to the ideal VIN_{-FS} + 0.5 LSB is applied at VIN1. R_{15} is then adjusted until the 0 to 1 transition occurs on the digital output. Finally, a voltage equal to the ideal VIN_{+FS} - 1.5 LSB is applied at VIN1. R_2 is then adjusted until the 255 to 256 transition occurs on the digital output.

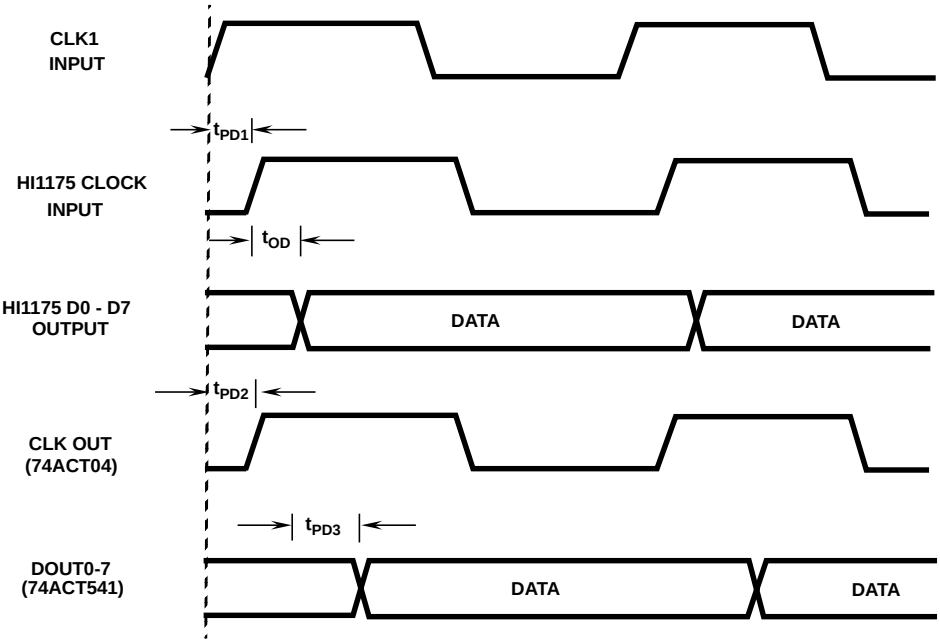


FIGURE 4. INPUT-TO-OUTPUT TIMING

Input Clock Driver and Timing

The input clock to the HI1175 evaluation board is a standard TTL clock applied to the CLK1 BNC. U4 (75ACT04) will buffer the clock and convert it to the CMOS levels necessary to drive the HI1175. For optimum performance of the HI1175 the duty cycle of the clock should be kept at 50%. U5 (74ACT541) will buffer the output bits and keep the power transients caused by charging a large buss capacitance off the supplies to the ADC.

TABLE 2. TIMING SPECS

PARAMETER	DESCRIPTION	MIN	TYP	MAX
t_{OD}	HI1175 Data Delay	-	18ns	30ns
t_{PD1}	74ACT04 Prop Delay	2.4ns	-	8.5ns
t_{PD2}	74ACT04 Prop Delay	2.4ns	-	8.5ns
t_{PD3}	74ACT541 Prop Delay	2.1ns	-	7.5ns

Figure 4 shows the timing for the evaluation board. The data corresponding to a particular sample will be available at the output of the HI1175 after the required data latency (2.5 cycles) plus an output delay. Table 2 lists the values that can be expected for the various timing delays. Refer to the datasheet for additional timing information.

HI1175 Characterization

Various tests can be used to characterize the performance of the HI1175. The integral nonlinearity (INL) and differential nonlinearity (DNL) specs are considered a measure of the low frequency characteristics of the ADC. These parameters are evaluated at the factory using a histogram approach with a low frequency ramp input.

A three bit reconstruction DAC, as shown in Figure 5, can be constructed to do a rough evaluation of HI1175 for DNL, missing codes, and transition noise.

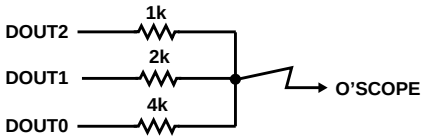


FIGURE 5. THREE BIT RECONSTRUCTION DAC

The input frequency is set so that the input will changes by 1 LSB for every k conversions of the ADC. The p-to-p voltage of the staircase is then determined by the number of LSB steps within one period of the input ramp.The following equations can be used:

$$V_{p-p} = \frac{m \times FSR}{2^n}$$

$$T = \frac{m \times k}{F_s}$$

Where:

F_S = sampling frequency of the ADC.

FSR = full scale range of the ADC.

k = desired test resolution (number of conversions per LSB).

m = desired number of steps (LSBs) per ramp period.

n = number of bits of the ADC.

For example, if k = 10, n = 8, m = 16, F_S = 20MSPS, and FSR = 1V then the input ramp would have a V_{P-P} of 62.5mV and a period (T) of 8µs. To view the reconstructed output, connect the X axis of an o'scope to the ramp input and the Y axis would be connected to the reconstruction DAC output. Another o'scope could be used to probe the bits to verify the codes that are being tested.The analog input should be low pass filtered to remove as much noise as possible. Notice that the input ramp is only covering m steps out a possible 2^n possible for the ADC. Therefore, the generator used for this test will have to be able to offset the input through the range of the converter so all the codes for the ADC can be inspected.

Figure 6 shows what an ideal reconstructed output would look like with and without various errors. For an ideal ADC and an ideal ramp input, the digital output code will change state by 1 LSB every kth conversion for an 1 LSB change on the input. ADC errors will make the codes change before or after the kth conversion and will translate to a larger or smaller step width. The actual step width size would be compared with the ideal LSB size to determine errors. Since this is a visual comparison it will tend not to be very precise.

Further dynamic testing is used to evaluate the HI1175 performance as the input starts to approach nyquist (F_S/2). Among these tests are Signal-to-Noise Ratio (SNR), Signal-to-Noise And Distortion (SINAD), and Total Harmonic Distortion (THD).

Coherent testing is recommended in order to avoid the inaccuracies due to windowing. Coherent sampling is governed by the following relationship: F_T/F_S = M/N. Where F_T is the frequency of the input tone, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and prime (1,3,5...) the samples are assured of being nonrepetitive.

Figure 7 shows the test system used to do dynamic testing on the HI1175. The clock (CLK) and analog input (AIN) signal sources are derived from low phase noise HP8662A generators that are phase locked to each other to ensure coherence. The output of the generator that drives the analog input to the evaluation board is first passed through a bandpass filter to improve the spectral purity of the signal. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has all the software to perform the Fast Fourier (FFT) and do the required data analysis.

A 12-bit accurate DAC is used to do the bandwidth testing. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The CLK and analog input frequencies are set up so a 1kHz beat frequency is generated on the

output of the DAC. Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output is 3dB down from the low frequency value.

Refer to the HI1175 datasheet for a complete list of test definitions and the results that can be expected using the evaluation board.

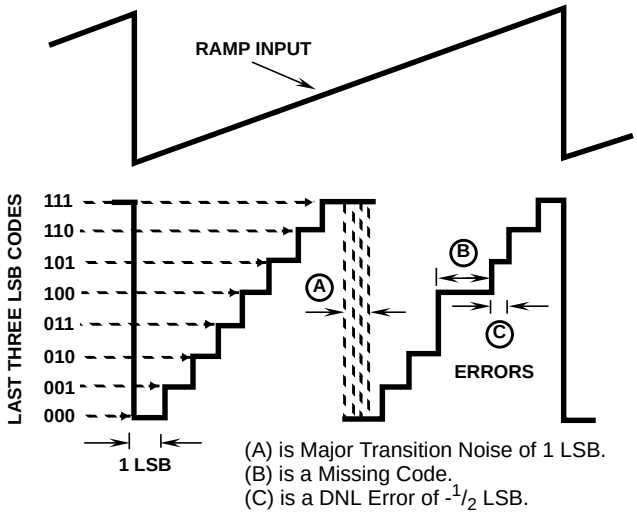


FIGURE 6. THREE BIT RECONSTUCTION DAC WAVEFORMS

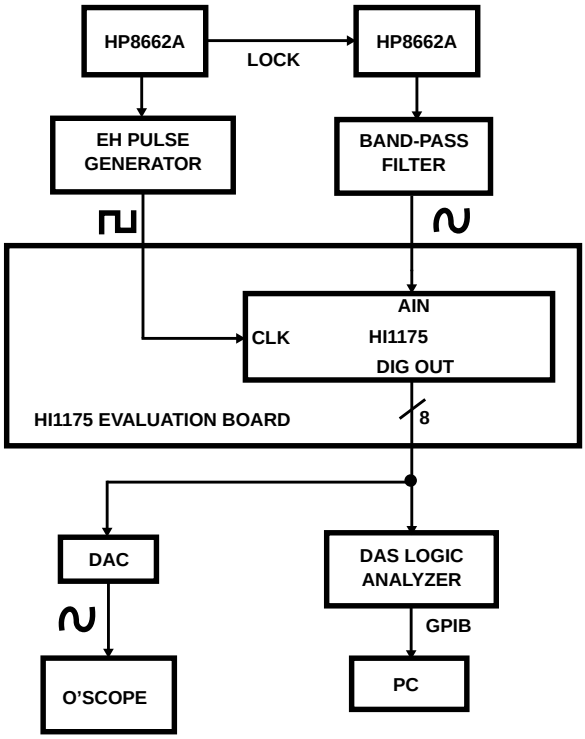


FIGURE 7. TEST SYSTEM

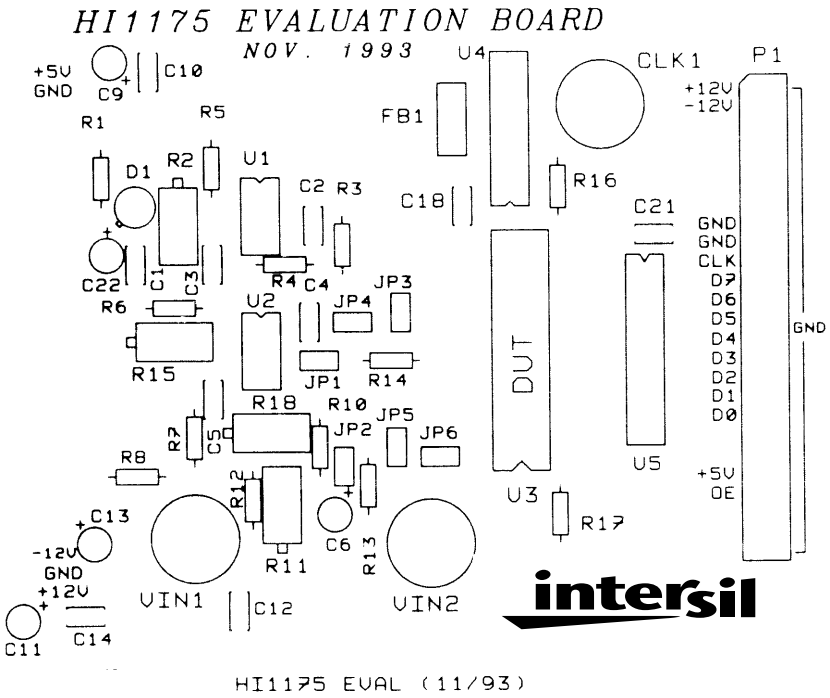


FIGURE 8. PARTS LAYOUT

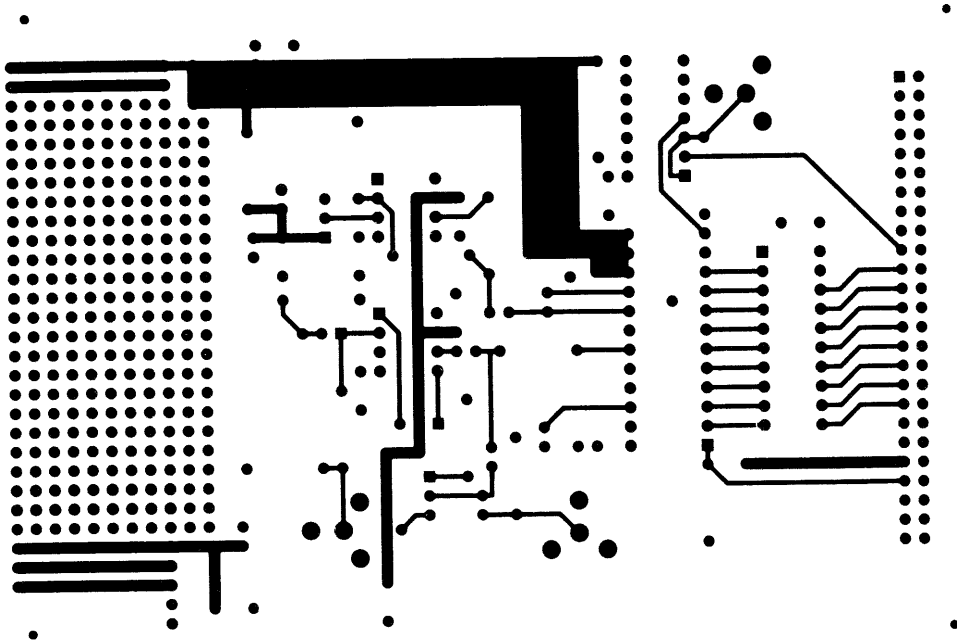


FIGURE 9. COMPONENT SIDE

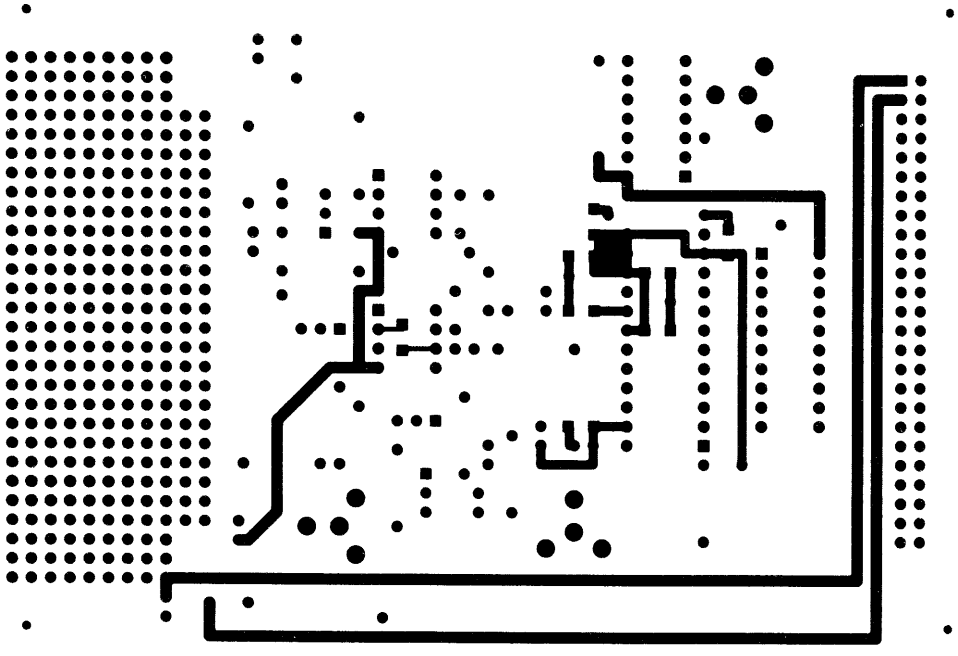


FIGURE 10. SOLDER SIDE

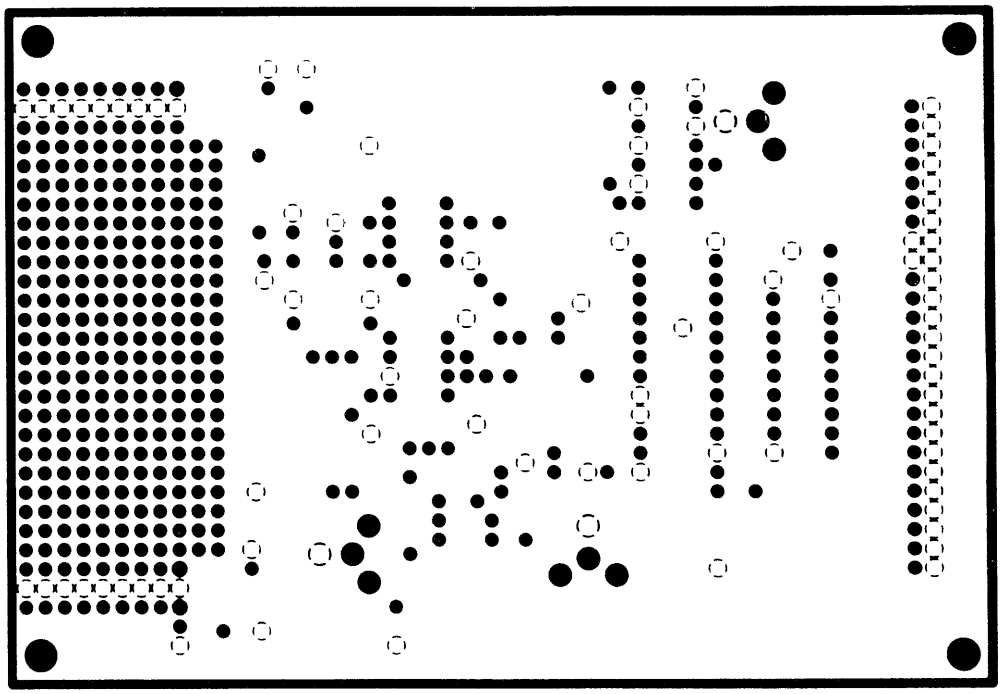


FIGURE 11. GROUND LAYER

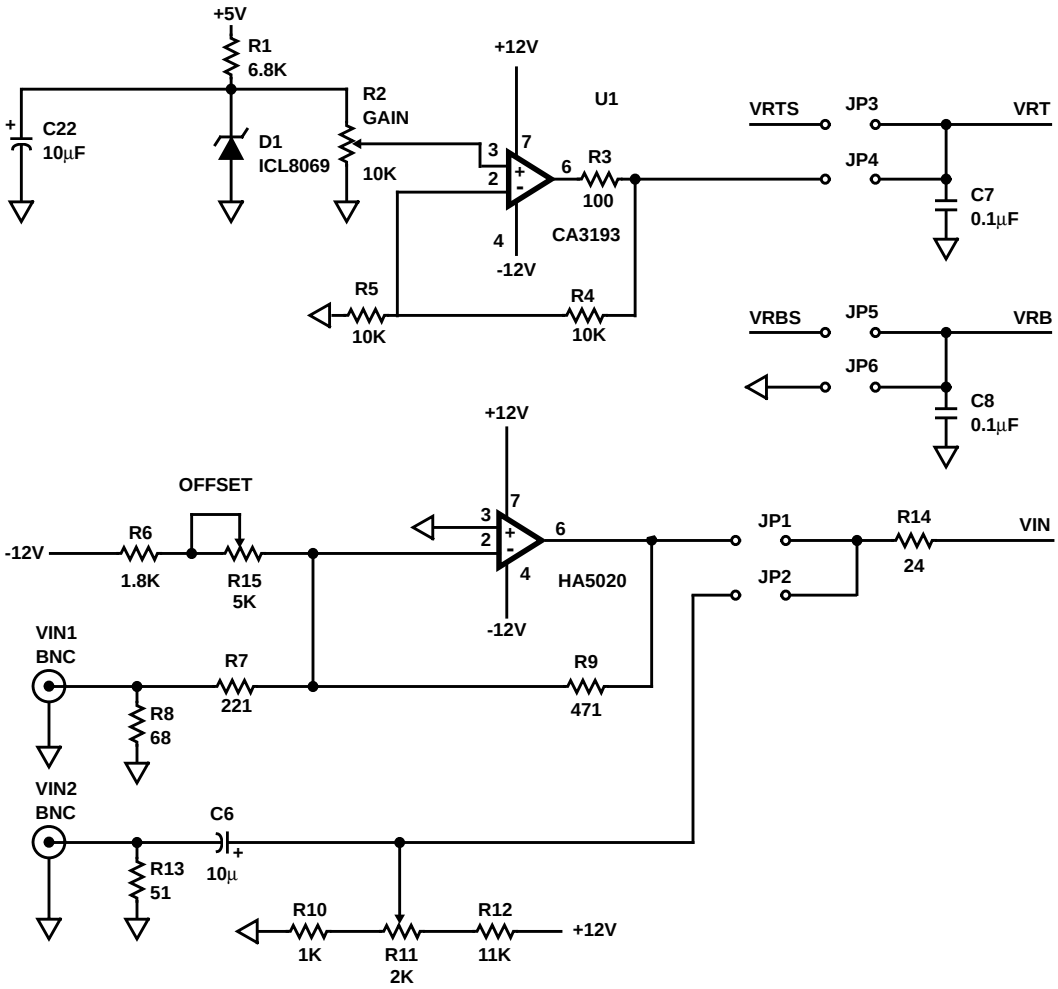


FIGURE 12. HI1175 EVALUATION BOARD

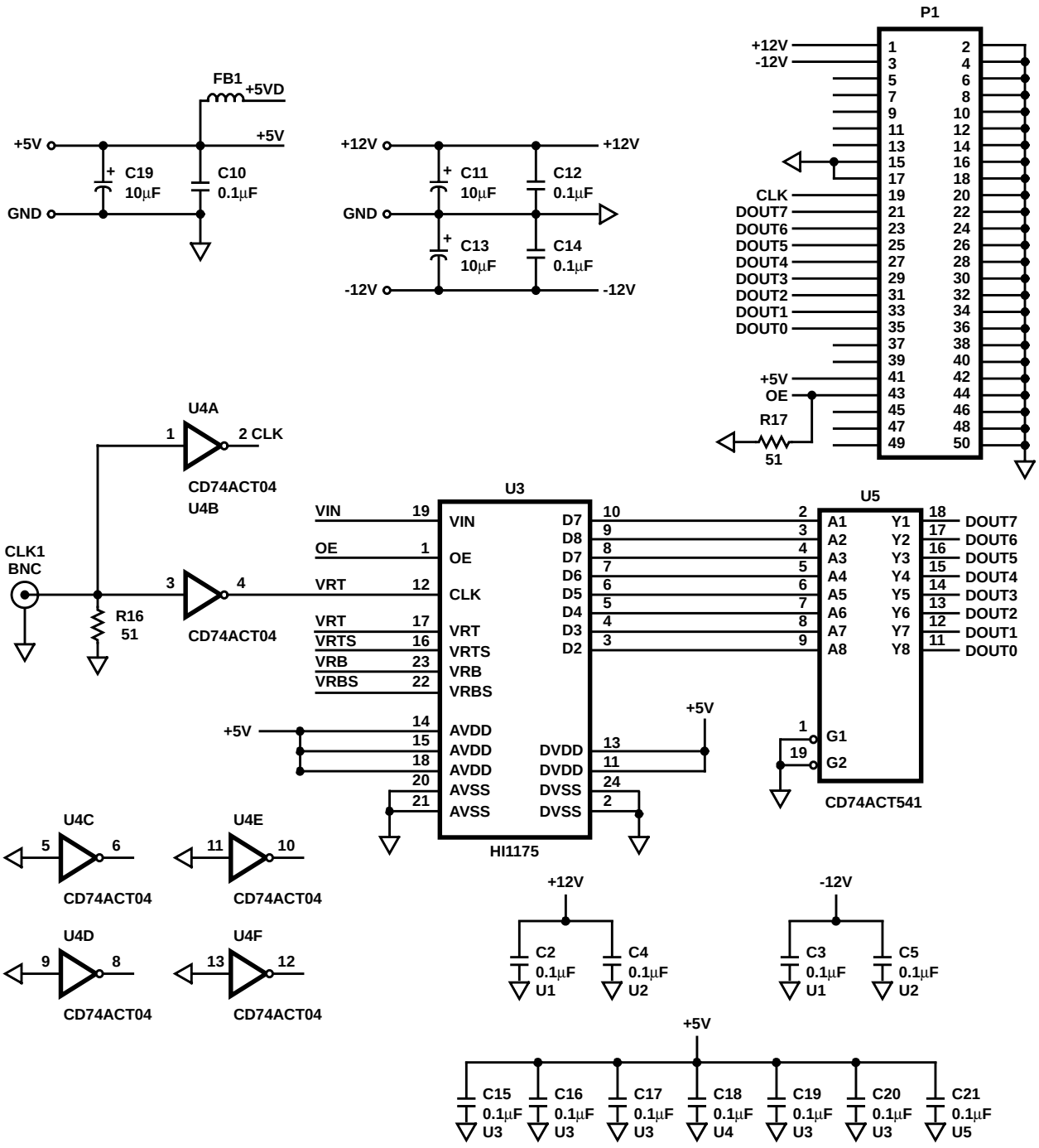


FIGURE 12. HI1175 EVALUATION BOARD (Continued)

Parts List for HI1175 Evaluation Board

DESIGNATOR	QUANTITY	DESCRIPTION
C15-C17, C7, C8, C20, C21	7	0.1µF 1206 CHIPS
C6, C9, C12, C13, C22	5	10µF TANT. 35WV
C2-C5, C10, C12, C14-C18, C20-21	14	0.1µF CKO5BX104K
C1	-	NOT INSTALLED
R1, R4, R5, R10	4	1K CARBON $^1/_8$W
R11	1	2K BOURNS POT
R12	1	11K CARBON $^1/_8$W
R13, R16, R17	3	51 CARBON $^1/_8$W
R14	1	22 CARBON $^1/_8$W
R15	1	5K BOURNS POT
R2	2	10K BOURNS POT
R3	1	100 CARBON $^1/_8$W
R6	1	1.8K CARBON $^1/_8$W
R7	1	221 METAL $^1/_4$W 1%
R8	1	68 CARBON $^1/_8$W
R9	1	471 1206 CHIP
R18	-	NOT INSTALLED

DESIGNATOR	QUANTITY	DESCRIPTION
VIN1, VIN2, CLK1	3	BNC STRAIGHT FEM
51	1	8 PIN SOCKET
53	1	14 PIN SOCKET
54	1	20 PIN SOCKET
J1-J6	6	SHUNTS
J1-J6	6	HEADERS
A/R	32	MINI SPRING SKT
P1	1	50 PIN HEADER
FB1	1	FERRITE BEAD
D1	1	ICL8069DCSQ
U1	1	CA3193E
U2	1	HA3-5020-5
U3	1	HI1175JCP
U4	1	CD74ACT04E
U5	1	CD74ACT541E

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